UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,645	11/21/2003	Jonathan H. Fischer	46-3	1260

47386 7590 07/24/2007

RYAN, MASON & LEWIS, LLP
1300 POST ROAD
SUITE 205
FAIRFIELD, CT 06824

EXAMINER	
MERCEDES, DISMERY E	
ART UNIT	**PAPER NUMBER**
2627	
MAIL DATE	**DELIVERY MODE**
07/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/719,645
Filing Date: November 21, 2003
Appellant(s): FISCHER ET AL.

Agere Systems, Inc.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 4, 2007 appealing from the Office action mailed May 2, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,111,467	Luo	8-2000
4,352,070	Beauducel et al.	9-1982

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 1, 7, 8 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Luo (US Patent No. 6, 111,467).

Regarding Claim 1, Luo teaches a sample and hold circuit having an input and an output, comprising: At least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output (See Element C1 in Fig. 1); At least one input switch for selectively connecting said at least one capacitive element to said input (See Fig. 1, Element S1); At least one output switch for selectively connecting said at least one capacitive element to said output (See Fig. 1, Element $3); And an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage (See Fig. 1, Element 11 and Col. 3, L. 50-64, wherein it teaches the amplifier having a reference or offset voltage in which it prevents that the voltage drop in the circuit will not be greater than the offset voltage. It is inherent to a person of ordinary skill to know that capacitors store voltage and hence, while the Element gm and switch S1 is conducting,

capacitor C1 will store a voltage offset produced by the circuit. See Col. 3, L. 45-50 and Col. 4, L. 5-10 and L. 33-35).

Method claim (8) is drawn to the method of using the corresponding apparatus claimed in claim (1). Therefore method claim (8) correspond to apparatus claim (1) and is rejected for the same reasons of anticipation as used above.

Regarding Claims 7 and 13, Luo teaches all the limitations of Claim 1 and 8, respectively. Luo further teaches that wherein limiting a voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit (It is inherent that because the voltage drop cannot be greater than the voltage offset, hence it reduces the leakage effect in the circuit by maintaining the voltage offset during the operation of the circuit.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luo in view of Beauducel et al (US Patent No. 4, 352,070).

Regarding Claims 4 and 11, Luo teaches all the limitations of Claims 1 and 8. However, although Luo discloses at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier to reduce leakage effects due to parasitic diodes in said at

least one of said input and output switches (see figs.2-3, wherein MOSFETs are being used as switches, and the leakage effect due to parasitic diode across the transistor is being reduced by maintaining a voltage offset in the circuit as discussed in claim 1 above.). Luo fails to specifically disclose wherein these switches are selectively connected in a hold mode or standard voltages in write mode. However, Beauducel et al. teaches two switches found between the input and output nodes in order to hold a voltage amount (See Col. 3, L. 1-20 of Beauducel et al.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Luo's invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

(10) Response to Argument

Claims 1 and 8

Applicant's arguments are fully considered but they are not persuasive. Regarding Claim 1 Applicant argues (1) Luo teaches away from the present invention by teaching to not limit a voltage drop across at least one the input and output switches to an offset voltage of an amplifier connected to the capacitive element (2) Applicant further agues that Luo does not disclose an amplifier connected to said node wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage. However, the examiner respectfully disagrees. Luo discloses at least one capacitive element for retaining charge (fig.1, element C1), said at least one capacitive element connected to a node between said input and said output (fig.1, C1 is connected to input and output of amplifier 11); at least one input switch for selectively connecting said at least one capacitive element to said input (fig.1, element S1, wherein the connection of capacitor C1 to input node, is based on whether switch S1 is open or closed); at

least one output switch for selectively connecting said at least one capacitive element to said output (fig.1, element S3, wherein the connection of capacitor C1 to output node, is based on whether switch S3 is open or closed); and an amplifier connected to said node (fig.1, element 11), wherein said amplifier has an offset voltage (fig.1, wherein capacitor C1 stores voltage offset when gm and switch S1 are conducting, see col.3, lines 45-50, col.4, lines 5-21 and 33-35) and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage (the voltage drop across input switch S1 is limited to the offset voltage when conducting, in coll.3, lines 50-64 is disclosed a voltage offset which prevents the voltage drop in the circuit will not be greater than the offset voltage, thus limiting the voltage drop; see also col.5, lines 27-45, wherein voltage Vx at the output is limited by offset voltage)

Regarding Claim 8, is a method claim drawn to the apparatus of claim 1, therefore is rejected for the same reasons of anticipation as discussed above in the rejection of claim 1.

Claims 7 and 13

Regarding Claims 7 and 13, Applicant Argues that Luo does not limit a voltage drop across at least one of the input and output switches to an offset voltage of an amplifier connected to the capacitive element, and wherein the limited voltage drop across at least one of the input and output switches reduces a leakage of the sample and hold circuit. However, the examiner respectfully disagrees. It is inherent that the voltage drop cannot be greater than the voltage offset, hence maintaining the voltage offset during operation of the circuit, thus limiting the voltage drop, reduces the leakage effect in the circuit.

Claims 4 and 11

Regarding Claims 4 and 11, Applicant Argues that the combination of Luo in view of Beauducel et al. does not disclose, at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches. However, the Examiner respectfully disagrees. Luo discloses at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches (see figs.2-3, wherein MOSFETs are being used as switches, and the leakage effect due to parasitic diode across the transistor is being reduced by maintaining a voltage offset in the circuit as discussed in claim 1 above. However, Beauducel et al. was relied upon to provide necessary teaching of two switches found between the input and output nodes in order to hold a voltage amount (See Col. 3, L. 1-20 of Beauducel et al.). Furthermore, Beauducel et al. is from the same field of endeavor, i.e. sample and hold circuit, and is properly combinable with Luo for providing the necessary teaching. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Luo's invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.)

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dismery Mercedes

Conferees:

ANDREA WELLINGTON
SUPERVISORY PATENT EXAMINER

Wayne Young
SPE